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PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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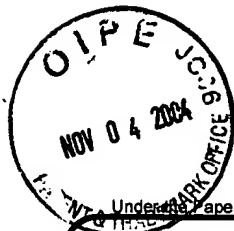
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/477,107	
	Filing Date	12/31/99	
	First Named Inventor	Christopher L. Hamlin	
	Group Art Unit	2131	
	Examiner Name	Dada, B. W.	
Total Number of Pages in This Submission		Attorney Docket Number	K35A0576

ENCLOSURES (check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an Application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Post Card
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Signature	
Date	11/1/04

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PTO/SB/17 (01-03)

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 340

Complete if Known

Application Number	09/477,107
Filing Date	12/31/99
First Named Inventor	Christopher L. Hamlin
Examiner Name	Dada, B. W.
Art Unit	2131
Attorney Docket No.	K35A0576

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☒ Deposit Account:Deposit Account Number
23-1209Deposit Account Name
WESTERN DIGITAL

The Commissioner is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) during the pendency of this application☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)					(\$)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	18.00	
Independent Claims		-3** =		X <th>84.00</th> <td></td>	84.00	
Multiple Dependent						

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1202	18	2202	9	Claims in excess of 20	
1201	84	2201	42	Independent claims in excess of 3	
1203	280	2203	140	Multiple dependent claim, if not paid	
1204	84	2204	42	** Reissue independent claims over original patent	
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2)					(\$)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for ex parte reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	340
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$) 340

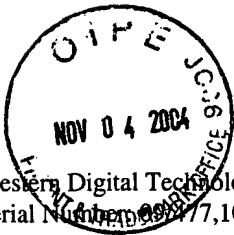
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Name (Print/Type)	Howard H. Sheerin	Registration No. (Attorney/Agent)	37,938	Telephone	303-765-1689
Signature	<i>Howard H. Sheerin</i>	Date	11/1/04		

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Western Digital Technologies, Inc.
Serial Number: 09477,107

1

Patent
Docket: K35A0576

In re Application of:
Christopher L. Hamlin
Serial No.: 09/477,107
Filed: 12/31/99
Title: INTEGRATED CIRCUIT COMPRISING
ENCRIPTION CIRCUITRY SELECTIVELY
ENABLED BY VERIFYING A DEVICE

Group Art Unit: 2131
Examiner: Dada, B. W.

BRIEF ON APPEAL

THE COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313

Sir,

The following appeal brief is submitted pursuant to the Notice of Appeal filed on
9/01/04, in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest for the above-identified patent application is Western Digital Technologies, Inc. (see assignment REEL/FRAME: 011959/0188 identifying Western Digital Technologies, Inc. as assignee of the entire right, title and interest of the above-identified patent application).

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences related to the instant appeal.

11/05/2004 HMEKONEN 00000037 231209 09477107

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STATUS OF CLAIMS

Claims 1-14 are the only claims pending and stand under final rejection. Claims 1-14 are the basis of this appeal.

STATUS OF AMENDMENTS

There are no outstanding amendments.

SUMMARY OF INVENTION

As illustrated in FIG. 1, the present invention may be regarded as an integrated circuit 100 for selectively encrypting plaintext data 102 received from a first device 104 to produce encrypted data 106 to send to a second device 108. The integrated circuit 100 comprises controllable encryption circuitry 110 comprising a data input 112, an enable input 114, and a data output 116. The integrated circuit 100 further comprises a plaintext input 118 for providing the plaintext data 102 to the data input 112, an encrypted text output 120 for providing the encrypted data 106 from the data output 116, and a first control input 122 for receiving a first device authentication signal 124 for authenticating the first device 104. A first verification circuit 130, responsive to the first device authentication signal 124, produces a first verification signal 132 for use in controlling the enable input 114 of the encryption circuitry 110 to enable the encryption circuitry 110 to provide the encrypted data 106 via the encrypted text output 120.

ISSUES

- I. Whether claims 1, 3-8 and 10-14 are patentable under 35 U.S.C. §103(a) over Brown et al. (5,892,826) in view of Lewis (5,734,819).

GROUPING OF CLAIMS

Claims 1-14 stand rejected and are grouped together for the purpose of this appeal.

THE REFERENCES

The following references are relied upon by the examiner:

Brown et. al.	5,892,826	April 6, 1999
Lewis	5,734,819	Mar. 31, 1998
Le Rue	5,694,469	Dec. 2, 1997

THE REJECTIONS

Claims 1, 3-8 and 10-14 stand rejected under 35 USC §103(a) as unpatentable over Brown et al. in view of Lewis. The examiner asserts that Brown discloses encryption circuitry but concedes that Brown does not teach to authenticate a device that provides plaintext data before enabling the encryption circuitry. The examiner asserts that Brown could be modified in view of Lewis to arrive at the claimed invention since Lewis discloses to authenticate a device using a unique chip identifier.

ARGUMENT

I. THE ISSUE UNDER 35 U.S.C. §103(a) – BROWN IN VIEW OF LEWIS

- A. The rejection should be reversed because modifying Brown in view of Lewis will not result in the claimed invention and therefore the examiner has failed to make a prima facie case of obviousness.

The rejection should be reversed because the examiner has failed to make a prima facie case of obviousness when the combination of references does not teach all of the claim limitations (MPEP 2143). In response to this argument, the examiner asserts the applicant is attacking the references individually rather than the combination. However, this interpretation of applicant's argument is incorrect. Modifying Brown in view of Lewis results in a combination that does not teach all of the claim limitations. It is only after the examiner interjects his own modifications in view of applicant's specification does the examiner arrive at all of the claim limitations.

The examiner concedes that Brown does not teach to authenticate a device before enabling an encryption circuit, but asserts that Lewis teaches this modification. However, Lewis discloses a system that authenticate a device before allowing software to run on the system (col. 5, lines 9-14). Therefore, modifying Brown in view of Lewis would result in a system that authenticates a device before allowing software to run on the system; it would not result in a system that authenticates a device before enabling encryption circuitry to operate as recited in the claims. Accordingly, the combination of references does not teach all of the claim limitations as required under MPEP 2143.

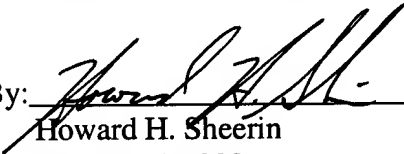
The suggestion to modify the prior art by authenticating a device before enabling encryption circuitry comes only from applicant's own disclosure which is not a proper basis to sustain a rejection under 35 USC §103.

CONCLUSION

Reversal of the rejections in this appeal is respectfully requested.

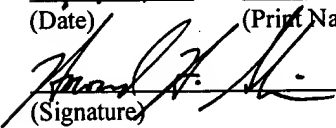
To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 23-1209, and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: 11/1/04 By: 
Howard H. Sheerin
Reg. No. 37,938
Tel. No. (303) 765-1689

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APPENDIX

A complete listing of the claims on appeal:

- 1 1. An integrated circuit for selectively encrypting plaintext data received from a first device
2 to produce encrypted data to send to a second device, the integrated circuit comprising:
3 controllable encryption circuitry comprising:
4 a data input;
5 an enable input;
6 a data output;
7 a plaintext input for providing the plaintext data to the data input;
8 an encrypted text output for providing the encrypted data from the data output;
9 a first control input for receiving a first device authentication signal for
10 authenticating the first device; and
11 a first verification circuit, responsive to the first device authentication signal, for
12 producing a first verification signal for use in controlling the enable input
13 of the encryption circuitry to enable the encryption circuitry to provide the
14 encrypted data via the encrypted text output.
- 1 2. The integrated circuit as recited in claim 1, further comprising:
2 a second control input for receiving a second device authentication signal
3 authenticating the second device;
4 a second verification circuit responsive to the second device authentication signal
5 for producing a second verification signal; and
6 a gating circuit responsive to the first and second verification signals for applying
7 an enable signal to the enable input to cause the controllable encryption
8 circuitry to provide the encrypted data via the encrypted text output.
- 1 3. The integrated circuit as recited in claim 1, wherein:
2 the first device authentication signal comprises a device identifier; and

3 the first verification circuit verifies the first device by comparing the device
4 identifier to a corresponding expected device identifier.

1 4. The integrated circuit as recited in claim 3, wherein the expected device identifier is
2 hardwired into the integrated circuit.

1 5. The integrated circuit as recited in claim 3, wherein:
2 the second device is a non-volatile memory; and
3 the expected device identifier is stored on the non-volatile memory.

1 6. The integrated circuit as recited in claim 1, wherein:
2 the first device authentication signal comprises a message authentication code
3 generated over the plaintext data using a device key; and
4 the first verification circuit verifies the first device by verifying the message
5 authentication code using an internal key.

1 7. The integrated circuit as recited in claim 1, wherein:
2 the first device is a signal processing circuit; and
3 the second device is a non-volatile memory.

1 8. A method of controlling encryption circuitry within an integrated circuit by selectively
2 encrypting plaintext data received from a first device to produce encrypted data to send to
3 a second device, the method comprising the steps of:
4 receiving the plaintext data from the first device;
5 receiving a first device authentication signal for authenticating the first device;
6 producing a first verification signal in response to the first device authentication
7 signal; and
8 enabling the encryption circuitry in response to the first verification signal to
9 provide the encrypted data to the second device.

- 1 9. The method of controlling encryption circuitry as recited in claim 8, further comprising
2 the steps of:
3 receiving a second device authentication signal authenticating the second device;
4 producing a second verification signal in response to the second device
5 authentication signal; and
6 enabling the encryption circuitry in response to the first and second verification
7 signals to provide the encrypted data to the second device.
- 1 10. The method of controlling encryption circuitry as recited in claim 8, wherein:
2 the first device authentication signal comprises a device identifier; and
3 the step of producing a first verification signal in response to the first device
4 authentication signal comprises the step of comparing the device identifier
5 to a corresponding expected device identifier.
- 1 11. The method of controlling encryption circuitry as recited in claim 10, wherein the
2 expected device identifier is hardwired into an integrated circuit.
- 1 12. The method of controlling encryption circuitry as recited in claim 10, wherein:
2 the second device is a non-volatile memory; and
3 the expected device identifier is stored on the non-volatile memory.
- 1 13. The method of controlling encryption circuitry as recited in claim 8, wherein:
2 the first device authentication signal comprises a message authentication code
3 generated over the plaintext data using a device key; and
4 the step of producing a first verification signal in response to the first device
5 authentication signal comprises the step of verifying the message
6 authentication code using an internal key.
- 1 14. The method of controlling encryption circuitry as recited in claim 8, wherein:
2 the first device is a signal processing circuit; and
3 the second device is a non-volatile memory.